CPU components and the fetch–decode–execute cycle

3.1.1b · Computers · revision notes

What the control unit, ALU, registers and clock do, what the address, data and control buses carry, and how they work together in the fetch–decode–execute cycle. Expect 1-mark recall, 4-mark 'Describe' questions on the stages of the cycle, 2-mark 'Explain' questions on clock speed and occasional address bus calculations on Paper 1.

Key facts

- CU: decodes instructions and sends control signals
- Registers: very small, very fast storage inside the CPU
- Address bus: memory addresses, CPU to memory only (one-way)
- Control bus: control signals such as read and write, both ways
- Grade 7+ only n-bit address bus → 2^n memory addresses
- ALU: arithmetic and logical operations, including comparisons
- Clock: regular pulses that keep the CPU in step; speed in Hz (1 GHz = 1,000,000,000 cycles per second)
- Data bus: data and instructions, both ways
- Cycle: fetch → decode → execute, then repeat

Notes

Inside the CPU

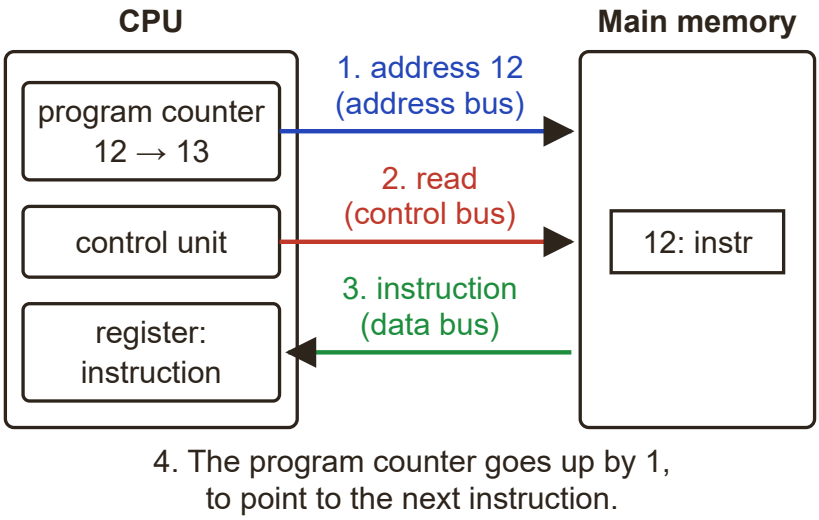
- **Control unit (CU)**: decodes each instruction and sends control signals (such as 'read' or 'write') to coordinate the other components.
- **Arithmetic logic unit (ALU)**: carries out arithmetic (such as adding and subtracting) and logical operations (such as AND, OR and comparisons like 'is A greater than B?').
- **Registers**: very small, very fast storage locations inside the CPU. They hold what the CPU needs straight away: the address of the next instruction, the current instruction, data being processed and results.
- Describe a register by what it holds. Two register names you may meet in questions are the **program counter** (holds the address of the next instruction) and the **accumulator** (holds results from the ALU).
- **Clock**: sends out regular electrical pulses that keep all the components in step. Clock speed is measured in hertz (Hz): 3 GHz = 3 billion cycles per second.

The three buses

- **Address bus**: carries the address of the memory location to be read from or written to. It is one-way: from the CPU to memory.
- **Data bus**: carries data and instructions between the CPU and memory. It is two-way.
- **Control bus**: carries control signals, such as read, write and clock signals. It is two-way.
- An n-bit address bus can address 2^n locations, so one extra wire doubles the number of addresses. A wider data bus moves more bits in one go. Grade 7+ only

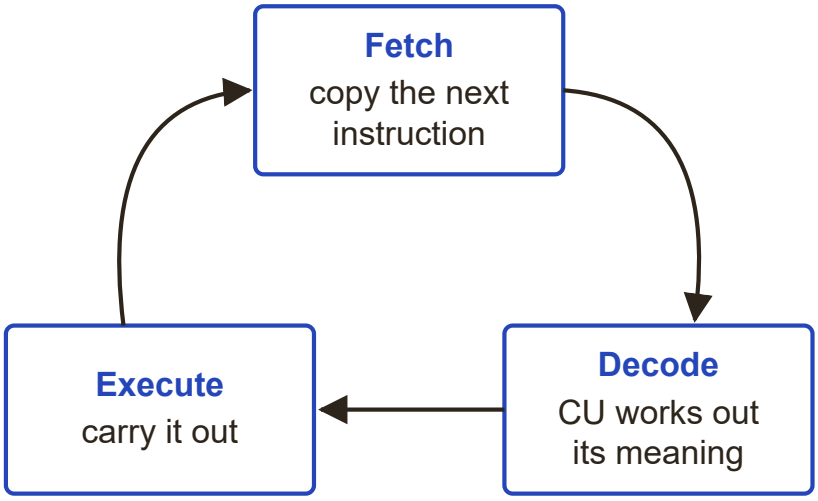
The fetch–decode–execute cycle

- **Fetch**: the address held in the program counter is sent along the address bus. The CU sends a read signal along the control bus. The instruction at that address comes back along the data bus and is stored in a register. The program counter is incremented so that it holds the address of the next instruction.



The fetch stage, step by step

- **Decode**: the CU works out what the instruction means: which operation to carry out and which data or address it uses.
- **Execute**: the instruction is carried out. For example, data is read from or written to memory, the ALU does a calculation and the result is stored in a register, or a jump changes the program counter.
- The cycle then repeats, billions of times a second.



The cycle repeats for every instruction, billions of times a second

Clock speed and performance

- A higher clock speed means more cycles each second, so more instructions can be fetched, decoded and executed each second.
- A faster clock makes the CPU produce more heat and use more power, which limits how fast it can be run.

How to answer each type of question

State the role of a CPU component or bus

1 mark each | Grade 4

1. Match the description to one component: decodes → CU; calculates or compares → ALU; tiny fast storage in the CPU → registers; regular pulses → clock.
2. Give one clear answer. Two different answers can lose you the mark.

Example. (a) State the purpose of the arithmetic logic unit (ALU). (1)
(b) State the purpose of the clock. (1)
(c) Identify the bus that carries 'read' and 'write' signals. (1)

Model answer.

(a) It carries out arithmetic and logical operations, e.g. adding two numbers or comparing them (1)
(b) It sends out regular pulses that keep the CPU's components in step (synchronised) (1)
(c) The control bus (1)

Describe the fetch stage

3 to 4 marks | Grade 6

1. Start with the address of the next instruction going along the address bus.
2. Mention the read signal on the control bus.
3. Say the instruction comes back along the data bus into a register.
4. Finish with the program counter being incremented.

Example. Describe what happens during the fetch stage of the fetch–decode–execute cycle. (4)

Model answer. Any four from: the address of the next instruction, held in the program counter, is sent along the address bus to main memory (1); the control unit sends a read signal along the control bus (1); the instruction stored at that address is sent to the CPU along the data bus (1); the instruction is stored in a register (1); the program counter is incremented so it holds the address of the next instruction (1).

Explain the effect of clock speed

2 marks | Grade 5

1. Say that a higher clock speed gives more clock cycles (pulses) per second.
2. Link it: so more instructions can be fetched, decoded and executed per second.

Example. Computer A has a clock speed of 2.4 GHz. Computer B has a clock speed of 3.6 GHz. Their CPUs are otherwise the same.
Explain why computer B is likely to run programs faster. (2)

Model answer. Computer B's clock produces more cycles (pulses) each second (1), so it can fetch, decode and execute more instructions each second (1).

Describe how a given instruction is decoded and executed

3 to 4 marks | Grade 7

1. Start with the control unit decoding the instruction: the operation and the address it uses.
2. Say which bus carries the address and which carries the data, and in which direction.
3. Say which control signal is sent (read or write).
4. Say where the result ends up.

Example. The accumulator is a register in the CPU. The instruction 'copy the value in the accumulator into memory address 50' has just been fetched.
Describe what happens during the decode and execute stages. (4)

Model answer. Any four from: the control unit decodes the instruction to find the operation (store) and the address (50) (1); the address 50 is sent along the address bus (1); the value in the accumulator is sent to memory along the data bus (1); the control unit sends a write signal along the control bus (1); the value is stored in memory location 50 (1).

Calculate with address bus width

1 to 2 marks | Grade 7

1. Work out 2^n, where n is the width of the address bus in bits: this is the number of memory locations.
2. Multiply by the size of each location (often 1 byte).
3. Divide by 1024 for each step up in units (bytes → KiB → MiB → GiB).

Example. A CPU has a 20-bit address bus. Each memory location holds 1 byte.
Calculate the maximum amount of memory, in MiB, that the CPU can address. (2)

Model answer.

2^{20} = 1,048,576 locations, so 1,048,576 bytes (1)
1,048,576 ÷ 1024 ÷ 1024 = 1 MiB (1)

Don't lose marks

- Saying the ALU decodes instructions. Decoding is done by the control unit.
- Saying the address bus is two-way, or that it carries data.
- Leaving out the step where the program counter is incremented.
- Writing 'the CPU gets the instruction from memory' without saying how (which bus, which signal). This is too vague for full marks.
- Confusing registers with RAM. Registers are inside the CPU and are much faster.
- Saying a higher clock speed makes 'the computer faster' without saying that more instructions are processed each second.

More tips

Memory tricks

- Order of the cycle: **F**etch, **D**ecode, **E**xecute. 'Friendly Dogs Eat.'
- In a fetch answer, name a bus in each step: address bus (where from), control bus (read), data bus (what comes back).
- Powers of 2 to know without a calculator: $2^{10} = 1024$, $2^{16} = 65{,}536$, $2^{20} = 1{,}048{,}576$. With 1 byte per location, a 20-bit address bus reaches 1 MiB and a 30-bit bus reaches 1 GiB.
- Giga means billion: 2.5 GHz = 2,500,000,000 cycles per second.

Exam technique

- For a 4-mark 'Describe', write the steps in order, with one marking point per sentence.
- Paper 1 has no calculator, so bus-width questions use powers of 2 you can work out by hand. Show each step.
- When a question gives you an instruction (such as 'add the value at address 21'), use its details: the operation, the address and where the result goes.
- Verbs examiners look for: sends, decodes, increments, executes, synchronises.

What each grade needs

What you need to be able to do, from the first marks up to the top grade.

Grade 3

Name the four main parts of the CPU

Control unit (CU), arithmetic logic unit (ALU), registers and clock.

Grade 4

State the role of each CPU component

The CU decodes and controls, the ALU calculates and compares, registers hold values and the clock keeps everything in step.

Grade 4

Put the stages of the cycle in order

Fetch, then decode, then execute, repeated for every instruction.

Grade 5

State what each bus carries, and which way

Address bus: addresses, one-way from the CPU; data bus: data and instructions, both ways; control bus: control signals, both ways.

Grade 5

Explain why a higher clock speed helps

More clock cycles each second means more instructions can be fetched, decoded and executed each second.

Grade 6

Describe the fetch stage step by step

Address out on the address bus, read signal on the control bus, instruction back on the data bus, program counter incremented.

Grade 7

Describe decoding and executing a given instruction

Say how the CU decodes it, which bus carries what, and what the ALU or memory does with it.

Grade 7

Calculate addressable memory from address bus width

An n-bit address bus can address 2^n memory locations.

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